## III. REMARKS

Claims 1-20 are pending in this application. Claims 1, 11, and 17 have been amended to provide improved clarity, and no claims have been cancelled. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the following remarks is respectfully requested.

Entry of this Amendment is proper under 37 C.F.R. § 1.116(b) because the Amendment: (a) places the application in condition for allowance as discussed below; (b) does not raise any new issues requiring further search and/or consideration; and (c) places the application in better form for appeal. Accordingly, Applicants respectfully request entry of this Amendment.

In the Office Action, claims 1-5, 7, 11-13, 15, 17, and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Su (U.S. Pub. 2006/0019482) in view of Cooney (U.S. Pub. 2004/0018714). With respect to claim 1, Applicants have amended claim 1 herein to provide improved clarity, but respectfully submit that Su and Cooney fail to teach each and every element of the claimed method. As noted in the Office Action (at page 3-4), Su fails to disclose the second through fourth steps in the order recited herein, comprising: deposition of a sacrificial layer which fails to substantially fill the opening, use of a directional etch on the sacrificial layer to form a sacrificial layer sidewall, and deposition of a conductive liner over the opening, between the not-yet-removed sacrificial sidewalls and the metal conductive lines (Claim 1, lines 4-8; *see also* Fig. 5).

Applicants respectfully submit that Cooney also fails to disclose a method including the

claimed steps. Specifically, Cooney does not teach a method including the sequential steps of depositing a conductive liner over the surface of sacrificial sidewalls, depositing metal in the opening, planarizing the metal and conductive liner, and finally, removing the sidewalls and covering the structure with a cap layer. In contrast with the claimed method, Cooney teaches the deposition of a sacrificial layer which does not substantially fill the opening 140 (see Fig. 18). The sacrificial layer then undergoes directional etching, removing the sacrificial layer from horizontal surfaces and forming sidewall spacers 141 (Fig. 19). After additional patterning to subsequently create vias 152a and 152b (Fig. 20), the sidewall spacers 141 are removed, and additional patterning forms vias 156a and 156b. As described in ¶ 0070, lines 6-8 *et seq.*, an optional conductive liner may then be deposited "prior to the copper fill material," in the space in vias 156a and 156b that the sacrificial sidewalls had previously occupied. As shown in Fig. 25, the vias, including the spaces formerly filled by the sidewall spacers 141, are then filled with metal. The conductive liner, if it is included, is situated between the metal conductive liner and the nitride, oxide, and dielectric layers. Sidewall spacers 141, born of sacrificial layer 140 and since removed, temporarily prevent sputtering onto the via bottom, and are removed before formation of the metal conductor lines. The space taken up by the sidewall spacers is subsumed into the resulting vias, and the resulting integrated circuit bears no evidence that Cooney's sidewall spacers 141 ever existed (Fig. 26). In contrast, the claimed method includes, *inter alia*, deposition of a sacrificial layer, which is not removed until the via is completely formed (*see* claims 1, lines 4-11; *accord* claims 11 and 17). The structure of the integrated circuit, less the air spacer itself, is completely formed before the sacrificial sidewalls are removed, and neither the vias nor the conductive liner occupy space previously occupied by the sacrificial sidewalls.

The conductive liner feature of the claimed invention (claim 1, line 8) is also specifically

not taught by either Su or Cooney. Su's method, as noted by the Office (at Office Action pp. 3-4) does not include a conductive liner at all, while Cooney includes an optional feature referred to as an "intermediate liner" (¶ 0070, line 7). This intermediate liner (Cooney, ¶ 0070, line 7) differs materially from the conductive liner of the claimed invention. The two liners are deposited in notably dissimilar steps. While the conductive liner feature of the claimed invention is deposited over the sacrificial sidewalls before their removal (*see* claim 1, lines 8-12, *accord* claims 11, 17), thus using the sidewalls to define the boundaries of the conductive liner, Cooney's intermediate liner is deposited in place of the sidewalls, after their removal (*see* ¶ 0070, lines 6-7 (describing the intermediate liner feature), *see also* Fig. 25). Cooney's method does not take advantage of (or acknowledge) the positive effect of air gaps on the edges of metal conductive lines to reduce the effective dielectric constant and thus decrease capacitative coupling between conductors, ultimately allowing for production of smaller semiconductor devices. Cooney's method is actually completely incompatible with exploiting this concept for improving semiconductor chip design. As the conductive liner feature of the claimed invention is not taught by either Su or by Cooney, Applicants respectfully submit that the claimed invention, including, *inter alia*, the conductive liner feature, is not obvious in view of Su and Cooney.

Applicants further submit that even if Su and Cooney were interpreted to teach each and every element of the claimed invention, a person with ordinary skill in the art would not be motivated to combine the teachings of Cooney and Su at the time the claimed invention was made. Applicants submit that it would not be possible to produce Su's interconnect structure (*see* Su, claims 25-27) or Su's structure of air gaps (*see* Su, claims 28-30) by applying the method of Cooney. Cooney does not contemplate the formation of air gap structures insulating a

contact via at all: instead, Cooney's use of a sacrificial layer improves contact interface properties in integrated circuits by preventing the laminated insulator stack from sputtering into the vias (claims 7, 15, 17), and by cleaning the vias and troughs (¶ 0011, lines 19-21). In dual damascene processing in soft non-silicon containing dielectrics, directional sputter cleans (such as traditional argon sputter cleans and reactive ion etching) often resputter polyarylenes (PAE) into the via bottom and onto the underlying metal, resulting in degraded contact interface properties. Cooney's sacrificial layer prevents PAE sputtering into the via bottom (Cooney, claims 7, 15, 17; *see also* ¶ 0013, lines 10-11) prior to the deposition of copper into the vias and troughs (¶ 0011, line 24), but is removed long before the metal conductive lines are fully formed.

Applicants also submit that it would be impossible to use the method of Su in combination with the method of Cooney, as the two methods comprise inherently incompatible intermediate steps. Su's method involves the formation of dielectric stakes 30, which are subsequently covered by sacrificial layer 50 which also substantially or completely fills the gaps between stakes (*see* Figs. 3-4). A hard mask layer is then formed above the sacrificial layer, and a patterned photoresist layer is formed above the hard mask layer (¶ 0025, lines 4-6; Fig. 4). Openings are then created according to the patterned photoresist layer using a dry etch through the sacrificial layer and the hard mask (¶ 0026, lines 1-4; Fig. 4), after which the photoresist layer and the horizontal surfaces of the sacrificial layer are removed by planarization (¶ 0026, lines 12-13; ¶ 0018, lines 2-4; Fig. 5). In contrast, Cooney uses a photoresist layer to pattern comparatively narrower vias (Figs. 15-16) and a sacrificial layer (conductive liner 140) is deposited which does *not* substantially fill the vias (Fig. 18). Rather than using a patterned photoresist layer and a dry etch process followed by planarization to etch the sacrificial layer as in Su, Cooney simply uses a directional etch to remove the sacrificial layer (conductive layer

140) from the horizontal surfaces of the structure (*see* Fig. 19). This technique is incompatible with the method of Su, because Su's sacrificial layer 50 is not exposed, but rather is covered by a hard mask layer, when the sacrificial layer is etched (Su, Fig. 4). Cooney's directional etch would not successfully remove the sacrificial layer in Su, nor would it be necessary, as Su provides for an alternative method in the patterned photoresist layer and a dry etch process.

For the above-stated reasons, Applicants submit that it would not have been obvious, nor was there motivation, to combine the teachings of Su and Cooney at the time of invention.

With respect to the rejections of independent claims 11 and 17, Applicants note that each claim includes features similar in scope to those already addressed above with respect to claim 1. Further, the Office relies on the same arguments and interpretations of Su and Cooney as discussed above with respect to claim 1. To this extent, Applicants herein incorporate the arguments presented above with respect to claim 1, and respectfully request withdrawal of the rejections of these claims for the above-stated reasons.

With respect to claims 2-5, 7, 12-13, 15, and 19, Applicants further respectfully submit that these dependent claims are allowable for reasons stated above relative to independent claims 1, 11, and 17, and for their own additional claimed subject matter. Accordingly, Applicants respectfully request that the Office withdraw the rejections under 35 U.S.C. § 103(a) to claims 2-5, 7, 12-13, 15, and 19.

In the Office Action, claims 8, 16, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Su and Cooney, and further in view of Cowley (U.S. Pub. 2004/0058526); claims 6, 14, and 18 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Su and Cooney, and further in view of Tsai (U.S. Pub. 2003/0077897); and claims 9 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Su and Cooney, and further in view

of Te Velde (U.S. Pat. 4,561,173). With respect to these eight dependent claims (6, 8-10, 14, 16, 18, and 20), Applicants respectfully submit that they are allowable for reasons stated above relative to independent claims 1, 11, and 17, and for their own additional claimed subject matter. Accordingly, Applicants respectfully request that the Office withdraw the rejections under 35 U.S.C. § 103(a) to claims 6, 8-10, 14, 16, 18, and 20.

## IV. CONCLUSION

Applicants respectfully submit that the Application as presented is in condition for allowance. Should the Examiner believe that anything further is necessary in order to place the application in better condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

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